Spider Tracks Limited

TEST REPORT FOR

Spider 7, Spider 7 Internal Antenna

Tested To The Following Standard(s)/Specification(s):
RTCA/DO-160G (2010)

Section: 17

Report No.: 97584-4

Date of issue: October 12, 2015

CKC Laboratories, Inc.

We strive to create long-term, trust based relationships by providing sound, adaptive, customer first testing services. We embrace each of our customers' unique EMC challenges, not as an interruption to set processes, but rather as the reason we are in business.

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ADMINISTRATIVE INFORMATION

Test Report Information

REPORT PREPARED FOR:	REPORT PREPARED BY:
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Representative: Sonja Ridder	Project Number: 97584

DATE OF EQUIPMENT RECEIPT: October 06, 2015
DATE(S) OF TESTING: October 06 - 07, 2015

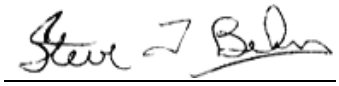
SCOPE: To demonstrate testing of the Spider 7, Spider 7 Internal Antenna meets the requirements for RTCA/DO-160G.

APPLICABLE DOCUMENTS:

- RTCA/DO-160G (December 8, 2010) Environmental Conditions and Test Procedures for Airborne Equipment.

Report Authorization

The test data contained in this report documents the observed testing parameters pertaining to and are relevant for only the sample equipment tested in the agreed upon operational mode(s) and configuration(s) as identified herein. Compliance assessment remains the client's responsibility. This report may not be used to claim product endorsement by A2LA or any government agencies. This test report has been authorized for release under quality control from CKC Laboratories, Inc.



Steve Behm
Director of Quality Assurance & Engineering Services
CKC Laboratories, Inc.

Test Facility Information

Our laboratories are configured to effectively test a wide variety of product types. CKC utilizes first class test equipment, anechoic chambers, data acquisition and information services to create accurate, repeatable and affordable test results.

TEST LOCATION(S):
CKC Laboratories, Inc.
22116 23rd Drive S.E., Suite A
Bothell, WA 98021-4413

Bothell - Semi-Anechoic Military/Aerospace EMC Chamber descriptions:

CKC Laboratories, Inc. operates three solid wall semi-anechoic chambers and one fully-anechoic chamber at their Bothell, Washington facility located in the Canyon Park business park. These chambers have attached solid wall ante-rooms for placement of support equipment and assisting in reducing ambient RF Emissions and RF leakage during RF susceptibility testing. The largest chamber does not have a solid wall ante-room.

Testing for this project was performed in the fully-anechoic C1 chamber. The dimensions of fully-anechoic chambers used for all Military/Aerospace EMC testing are as follows:
CP-C1: Chamber is 30'w x 16'd x 11'h

The shielded enclosures are designed to attenuate radio frequency noise over 100 dB up to 1GHz, and over 70 dB up to 40GHz.

The walls and ceiling of the semi-anechoic chambers have been treated with RF absorbing ferrite tiles and 1 foot RF absorbing cones in order to achieve uniform RF absorption from 10MHz to 40GHz. The minimum absorption performance at normal incidence exceeds the requirements of DO-160F Section 20 paragraph 20.3.b.(5) and table 20-3 as shown below:

10MHz	≥9dB	425MHz	≥38dB
80MHz	≥17dB	1GHz	≥25dB
250MHz	≥27dB	40GH	≥30dB

All input power to the room is filtered at its point of entry. The filters provide 100dB of insertion loss over the frequency range of 10kHz to 40GHz.

Ground Plane descriptions:

The ground plane used for all EMC testing is bonded to a wooden test bench. The dimensions are as follows:
CP-C1: 12' long x 3.5' deep x 0.025" thick copper bonded to bench surface.

The ground planes are bonded to the shielded enclosure wall at a minimum of once every 20 inches using copper bonding straps 12" in length x 4" in width exceeding the 5:1 length to width ratio requirements of DO-160F Section 20 para 20.3.a.(1).

Software Versions

CKC EMITest Emissions: 5.02.00
CKC Immunity: 5.02.00
NEXIO BAT-EMC: 3.10.0.14

UNIT UNDER TEST (UUT) DESCRIPTION

The Spider 7 contains the PCB Board listed below.

UNIT UNDER TEST

Spider 7
Manuf: Spider Tracks Limited
Model: Spider 7 Internal Antenna
Serial: 2015BETA33

PCB Board
Manuf: Spider Tracks Limited
Model: V3.5
Serial: N/A

PERIPHERAL DEVICES

The UUT was not tested with peripheral devices.

Mode / Configuration

Mode/Configuration Definitions	
Mode/Configuration	**Definition/Description**
1	Transmitting location data via Iridium. Bluetooth low energy transmitter is operational

SUMMARY OF RESULTS

Standard / Specification: RTCA/DO-160G

Test Description	Results	Category	Outcome
17 - Voltage Spike	No degradation of performance was found during the extent of testing at $56V_{pk}$.on the 28VDc Input Power Lead.	**B**	**PASS**

Bonding Resistance Measurements

Bonding Resistance Measurements:
UUT was isolated 5cm above the EMI Ground Plane, therefore no Bonding Resistance Measurements were required.

RTCA/DO-160G

Section 17 – Voltage Spike Category B

Test Equipment					
Asset	**Description**	**Manufacturer**	**Model**	**Cal Date**	**Cal Due**
01577	Generator,Transient Pulse - Spike	Solar	8282-1	05/08/15	05/08/17
01575	Pulse Transformer, 50 Ohm Transient	Solar	8527-1	05/08/15	05/08/17
P06031	Feed Through Capacitor	Solar	6512-106R	03/21/14	03/21/16
03369	Probe, HV	Tektronix	P5100A	03/26/15	03/26/17
03516	Oscilloscope	Tektronix	TDS3052	11/25/14	11/25/16

Spec Limit: RTCA/DO-160G Section 17, Category B.

Test Procedure

The output of the 50Ω source impedance voltage spike generator was adjusted to produce the required peak voltage 10uS spikes in accordance with RTCA/DO-160G Section 17 Figure 17-1. The source impedance of the voltge spike generator was verified by placing a 50Ω load across the output of the generator, and observing that the amplitude was reduced to 50% of the calibration level.

The UUT was installed into the circuit by connecting the power lead of the UUT in series with the coupling transformer. One transient pulse per second was injected onto the power lines. After pulses were injected for 1 minute at a minimum rate of 1 pulse per second, the amplitude was reduced and the UUT was turned off. The output of the spike generator was reversed and the test was repeated as described above in negative polarity. The UUT was monitored throughout the testing and its functionality was verified after the testing was completed. Test was repeated for each lead listed in the table below.

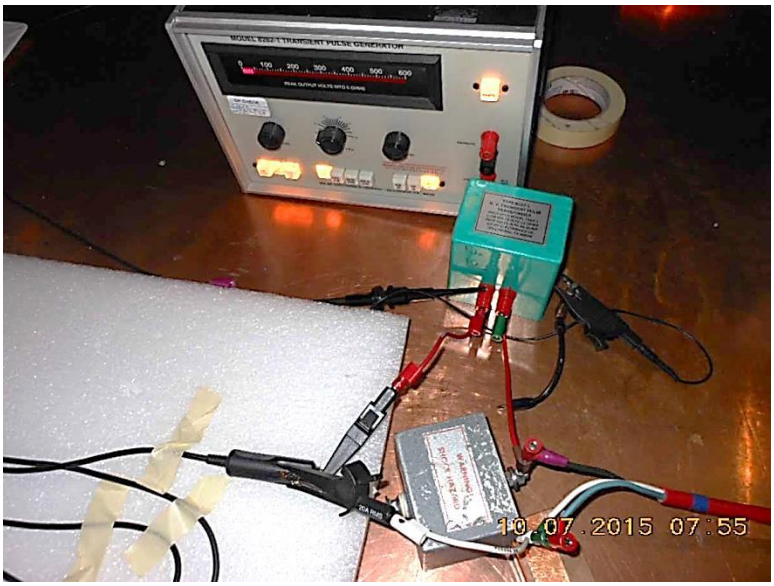
Test Results						
Mode/Config #	**Lead Tested**	**V pk**	**Pulses Applied**	**Polarity**	**Results**	**Observations**
1	+28Vdc	56V	50	Positive	PASS	
1	+28Vdc	56V	50	Negative	PASS	

Section 17 Voltage Spike Test Setup Photos

Section 17 – Calibration Setup, Open Circuit

Section 17 – Calibration Setup, 50 Ohm

Section 17 – Overall View of Test Setup

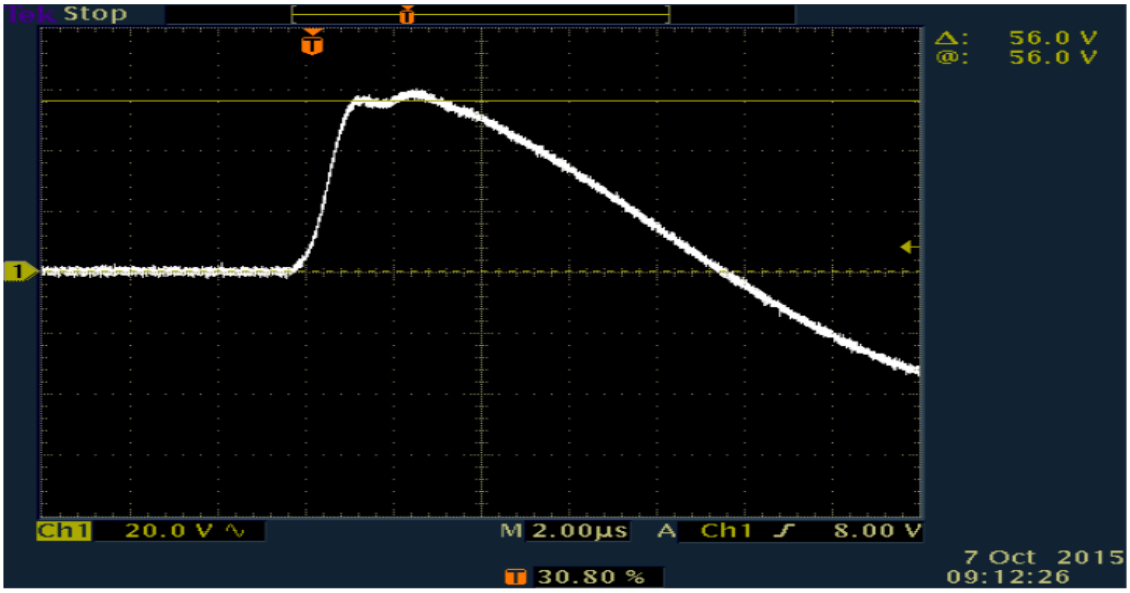


Section 17 –Close-up

Section 17 Voltage Spike Category B Test Data

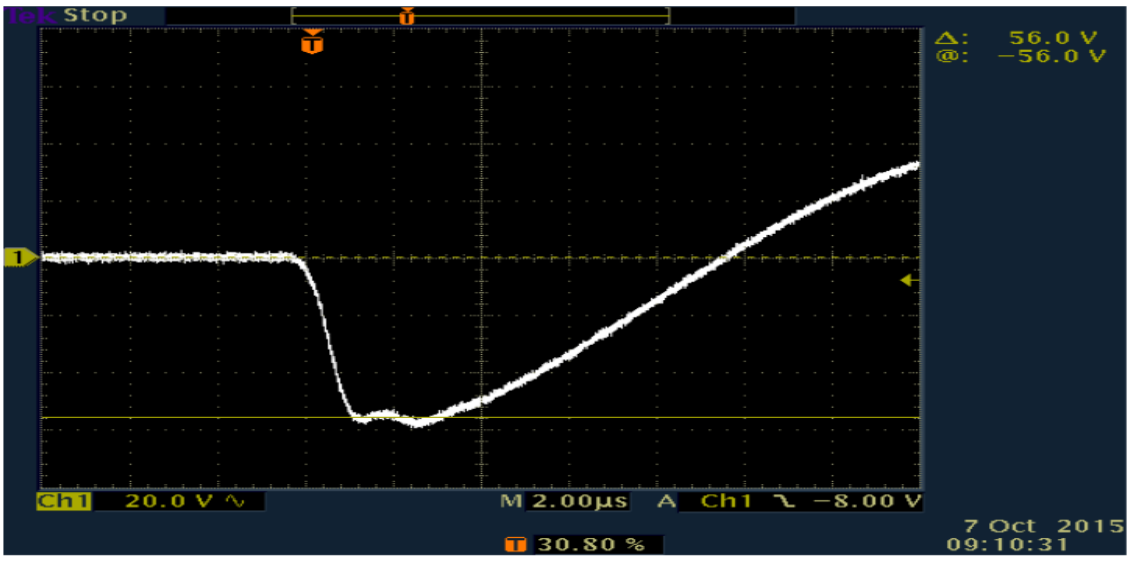
S/N 2015BETA33 Eng.: S. Pittsford Tested: 10/07/15

This waveform capture shows the positive polarity open circuit calibration voltage of the voltage spike transient.



TDS 3052 - 9:21:18 AM 10/7/2015

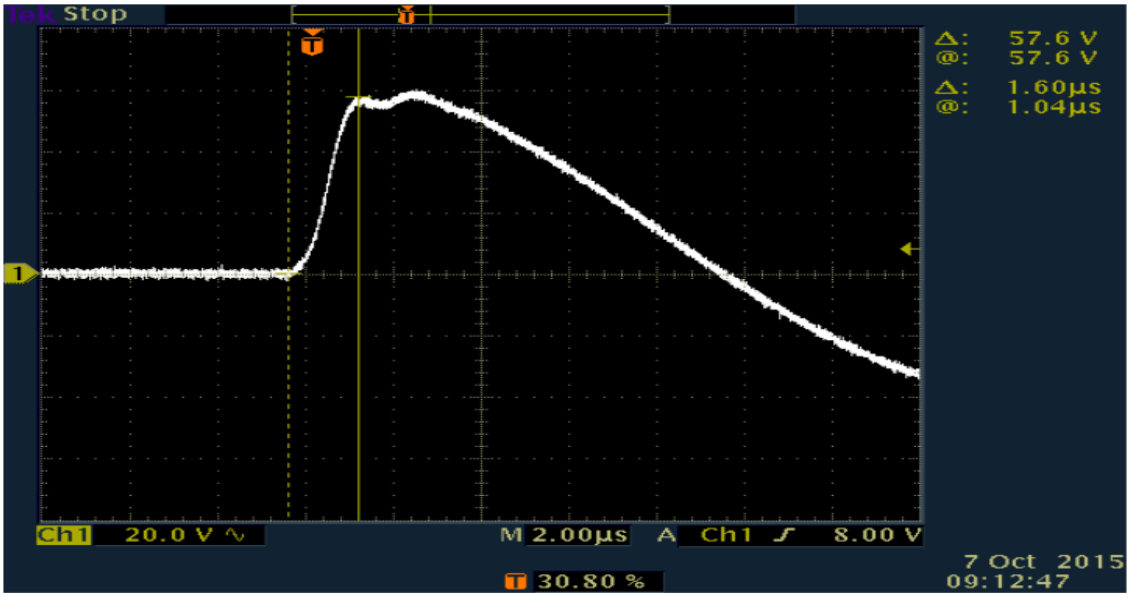
This waveform capture shows the negative polarity open circuit calibration voltage of the voltage spike transient.



TDS 3052 - 9:19:24 AM 10/7/2015

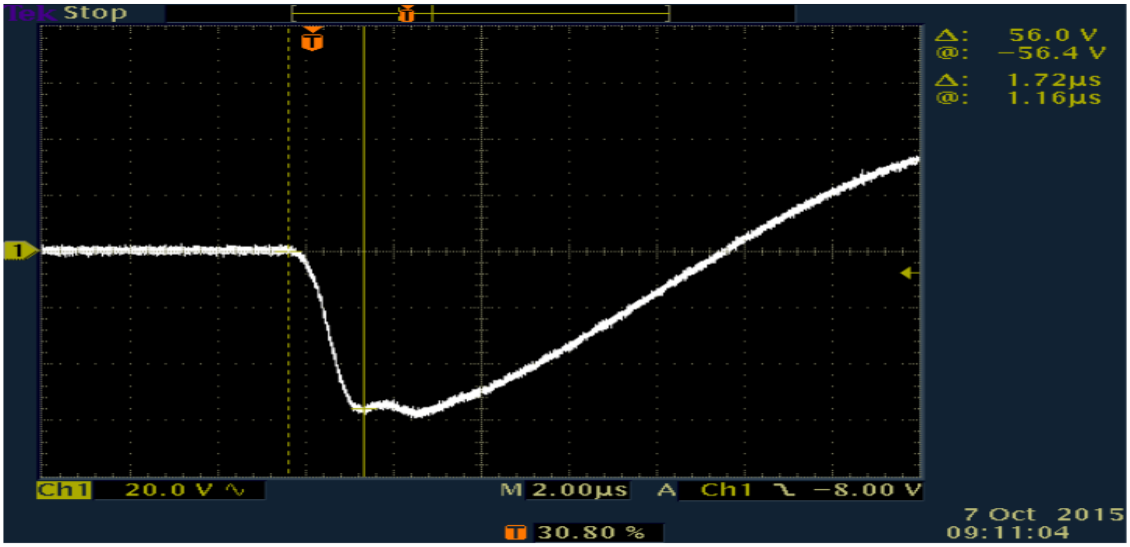
DO-160G Section 17 Voltage Spike – CAT B

This waveform capture shows the positive polarity open circuit calibration voltage of the voltage spike transient rise time.



TDS 3052 - 9:21:39 AM 10/7/2015

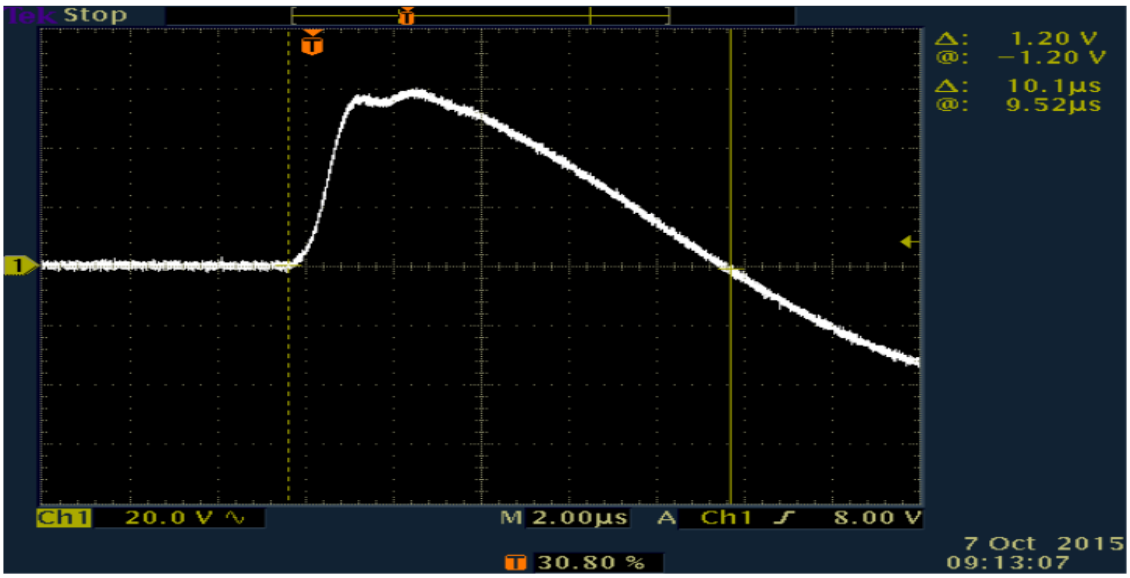
This waveform capture shows the negative polarity open circuit calibration voltage of the voltage spike transient rise time.



TDS 3052 - 9:19:57 AM 10/7/2015

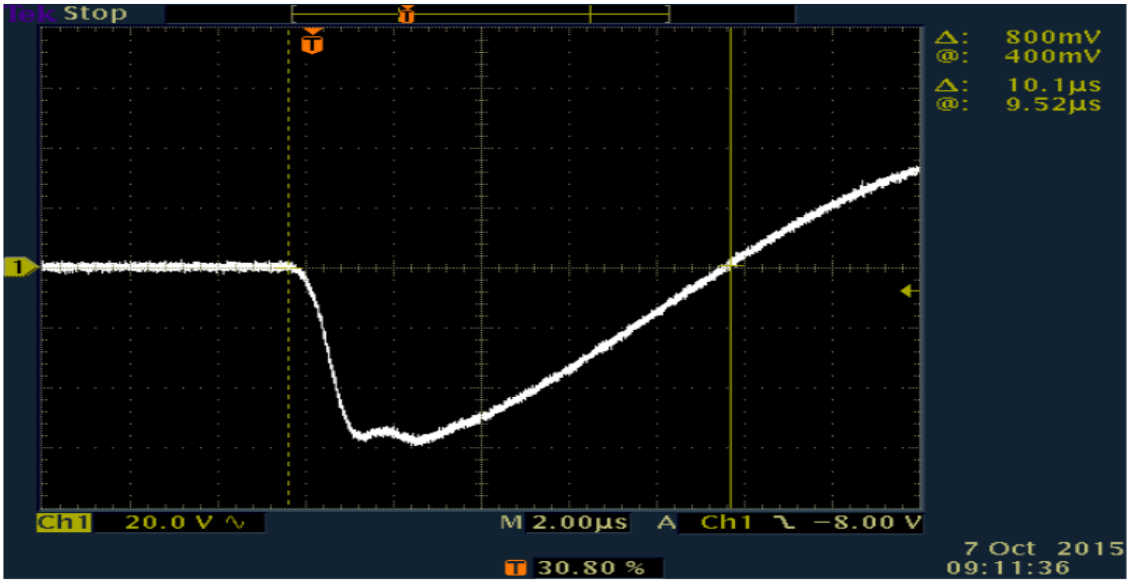
DO-160G Section 17 Voltage Spike – CAT B

This waveform capture shows the positive polarity open circuit calibration voltage of the voltage spike transient pulse width.



TDS 3052 - 9:21:59 AM 10/7/2015

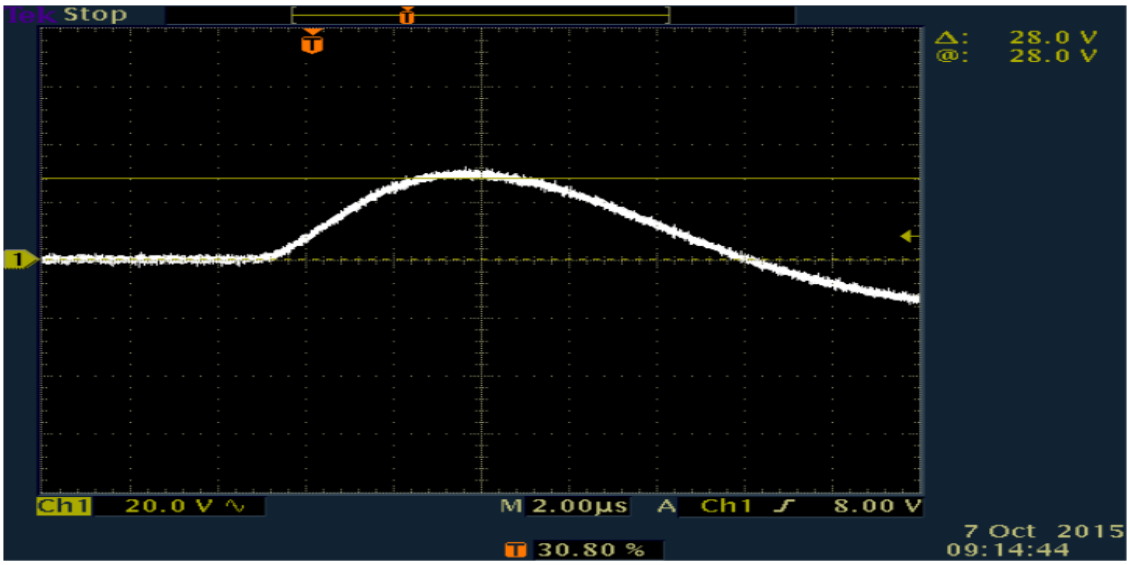
This waveform capture shows the negative polarity open circuit calibration voltage of the voltage spike transient pulse width.



TDS 3052 - 9:20:29 AM 10/7/2015

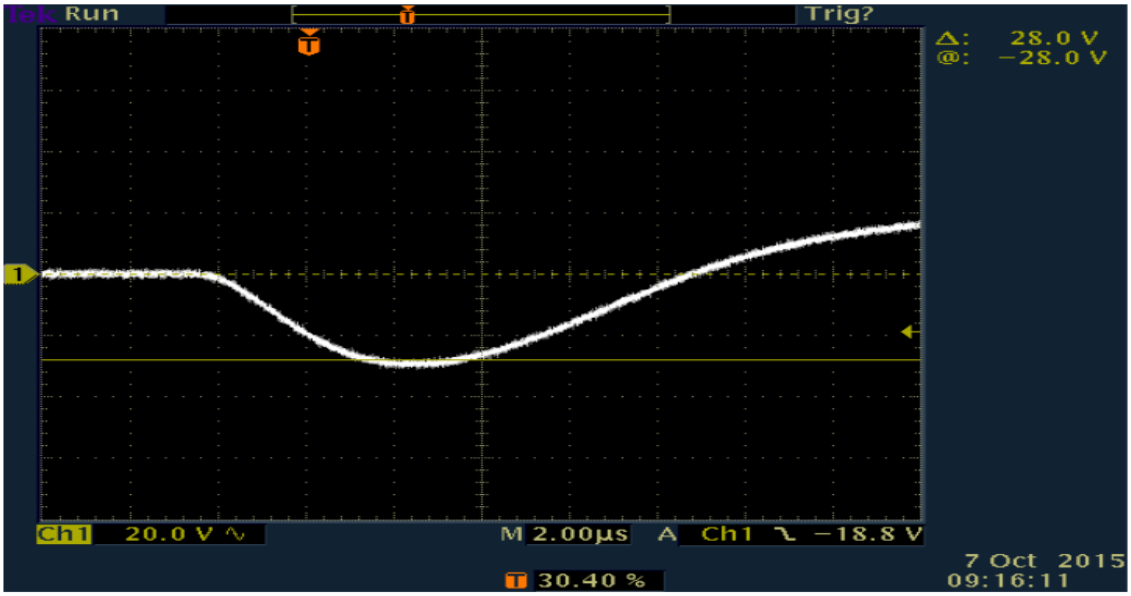
DO-160G Section 17 Voltage Spike – CAT B

This waveform capture shows the ½ amplitude positive polarity 50Ω source impedance calibration voltage of the voltage spike generator with a 50Ω load across the output terminals of the generator.



TDS 3052 - 9:23:36 AM 10/7/2015

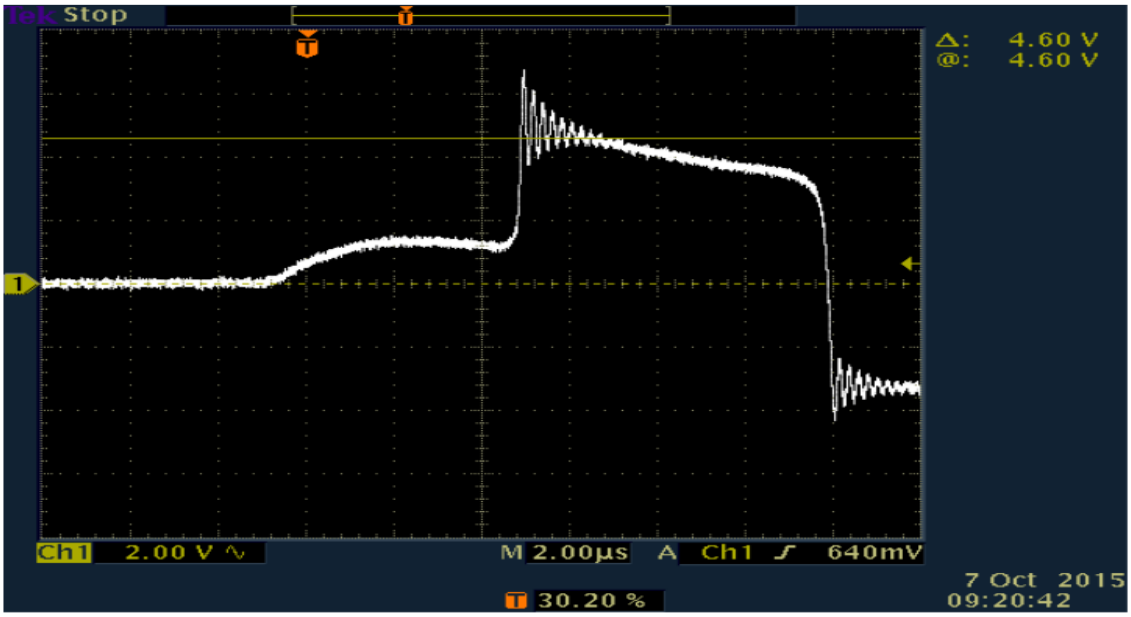
This waveform capture shows the ½ amplitude negative polarity 50Ω source impedance calibration voltage of the voltage spike generator with a 50Ω load across the output terminals of the generator.



TDS 3052 - 9:25:03 AM 10/7/2015

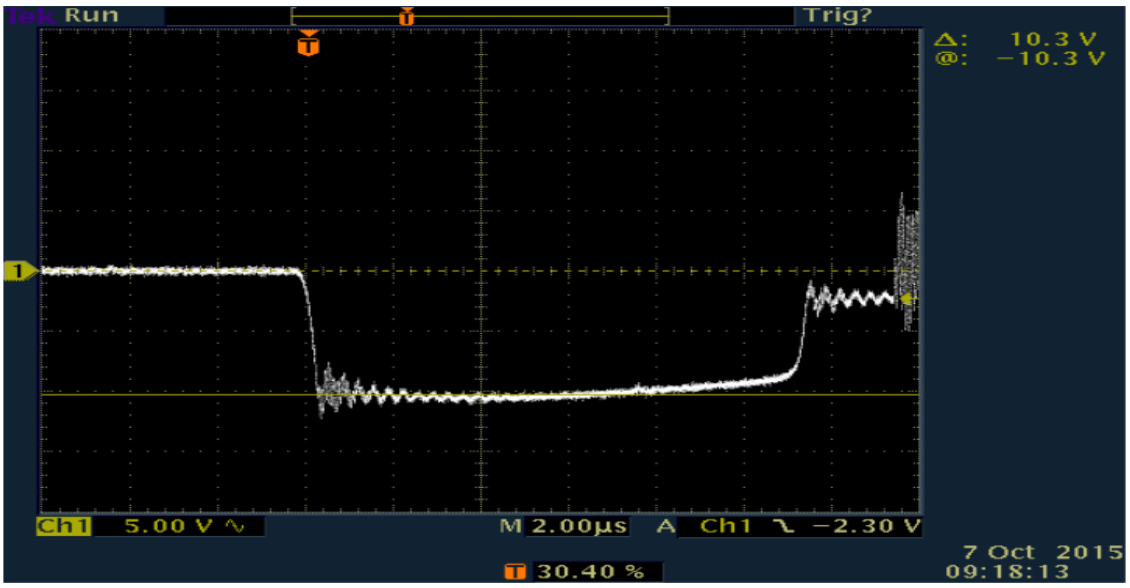
DO-160G Section 17 Voltage Spike – CAT B

This waveform capture shows a typical positive polarity voltage spike transient applied to the UUT.



TDS 3052 - 9:29:34 AM 10/7/2015

This waveform capture shows a typical negative polarity voltage spike transient applied to the UUT.



TDS 3052 - 9:27:05 AM 10/7/2015

TEST LOG

Date	Name	Time	Event
10/7/15	S. Pittsford	0730	**Section 17 - Voltage spikes CAT B** No degradation observed
		0900	Done with DO-160G Testing